lococube® STG-Series miCon-L Firmware

CHANGELOG

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OVERVIEW

Status: *active*
- STG-800/810
- STG-820
- STG-850

Status: *active (no further development)*
- STG-580
- STG-680
- STG-700

Status: *obsolete (no further development/maintenance)*
- STG-32
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- STG-500/501
- STG-550/570
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- STG-650
- STG-860

Last Update: ***17 December 2021***

STG-32 (OBSOLETE)

V1.0.4.0 (2016-10-19)
- New: reset circuit to clear the program
- Known issue: Timer racing condition - Bug (with 16Bit controller): Clock generator issues no pulse for 66 seconds if the CG block (clock generator) is interrupted exactly while reading the system time stamp by the timer interrupt

V1.0.3.0 (2016-05-09)
- 1. Release
- PWM up to 32500Hz

STG-115 (OBSOLETE)

V1.0.2.0 (2015-09-17)
- 1. Release
- Known issue: Timer racing condition - Bug (with 16Bitcontroller): Clock generator issues no pulse for 66seconds if the CG block (clock generator) is interruptedexactly while reading the system time stamp by the timer interrupt

STG-500/501 (OBSOLETE)

V5.0.3.0 (2016-10-19)
- New: reset circuit to clear the program
- Known issue: Timer racing condition - Bug (with 16Bit controller): Clock generator issues no pulse for 66 seconds if the CG block (clock generator) is interrupted exactly while reading the system time stamp by the timer interrupt

V5.0.2.0 (2016-08-05)
- New: continuously calculation of the ADC value (blocks take the value from the chart)
- Improvement: accuracy of the timer
- Improvement: accuracy of the fast counters
- Change: remanence block writes only in the event of a change

V5.0.1.0 (2014-11-18)
- Bugfix: base timer

V5.0.0.1 (2014-02-11)
- Change: voltage divider for the calculation of the ADC voltage

V5.0.0.0 (2012-11-16)
- 1. Release

STG-550/570 (OBSOLETE)

V1.0.4.0 (2016-10-19)
- New: reset circuit to clear the program
- Known issue: Timer racing condition - Bug (with 16Bit controller): Clock generator issues no pulse for 66 seconds if the CG block (clock generator) is interrupted exactly while reading the system time stamp by the timer interrupt

V1.0.3.1 (2016-08-09)
- Bugfix: converter (float in ..) (Only exists for V1.0.3.0)

V1.0.3.0 (2016-08-05)
- New: continuously calculation of the ADC value (blocks take the value from the chart)
- New: block for the measurement of the CPU load
- Improvement: accuracy of the timer
- Improvement: accuracy of the fast counters
- Change: remanence block writes only in the event of a change

V1.0.2.1 (2016-03-11)
- Bugfix: Watchdog (Controllers performed a reboot after one hour, but continue normally now)

V1.0.2.0 (2015-11-19)
- Change: adaption of the hardware with revision B (external reference for voltage measurement)

V1.0.1.0 (2015-10-23)
- New: support of the CAN layer 2 library V2.0 with 29-bit identifier

V1.0.0.2 (2015-10-19)
- Bugfix: PWM duration

V1.0.0.1 (2015-09-23)
- 1. Release

STG-580 (ACTIVE – NO DEVELOPMENT)

V1.0.1.2 (2017-10-27)
- New: clock generator 2 (Bugfix for clock generator 1 with slightly changed behavior in macros with the ENABLE block)
- New: Modbus: enhanced setting possibility for parity and number of stop bits (A parity check on the reception does not take place)
- Short flashing of the status LED during power up (on for the duration of initialization)
- Known issue: Timer racing condition - Bug (with 16Bit controller): Clock generator issues no pulse for 66 seconds if the CG block (clock generator) is interrupted exactly while reading the system time stamp by the timer interrupt

V1.0.1.1 (2017-08-09)
- Bugfix: Modbus: multi-slave nets are possible now

V1.0.1.0 (2016-10-19)
- New: reset circuit to clear the program

V1.0.0.1 (2016-08-09)
- Bugfix: converter (float in ..)

V1.0.0.0 (2016-08-03)
- 1. Release

STG-600 (OBSOLETE)

V1.0.1.0 (2016-08-05)
- New: continuously calculation of the ADC value (blocks take the value from the chart)
- New: block for the measurement of the CPU load
- Improvement: accuracy of the timer
- Improvement: accuracy of the fast counters
- Change: remanence block writes only in the event of a change
- Known issue: Timer racing condition - Bug (with 16Bit controller): Clock generator issues no pulse for 66 seconds if the CG block (clock generator) is interrupted exactly while reading the system time stamp by the timer interrupt

V1.0.0.5 (2013-12-03)
- Bugfix: allocation

V1.0.0.4 (2013-11-05)
- Bugfix: float converter

V1.0.0.3 (2013-10-29)
- Bugfix: converter library added

V1.0.0.0 (2013-10-21)
- 1. Release

STG-606 (OBSOLETE)

V1.0.2.0 (2016-10-19)
- New: reset circuit to clear the program
- Known issue: Timer racing condition - Bug (with 16Bit controller): Clock generator issues no pulse for 66 seconds if the CG block (clock generator) is interrupted exactly while reading the system time stamp by the timer interrupt

V1.0.1.0 (2015-10-23)
- New: support of the CAN layer 2 library V2.0 with 29-bit identifier

V1.0.0.1 (2015-09-23)
- 1. Release

STG-650 (OBSOLETE)

V1.0.4.0 (2016-10-19)
- New: reset circuit to clear the program
- Known issue: Timer racing condition - Bug (with 16Bit controller): Clock generator issues no pulse for 66 seconds

V1.0.3.1 (2016-08-09)
- Bugfix: converter (float in ..) (Only exists for V1.0.3.0)

V1.0.3.0 (2016-08-05)
- New: continuously calculation of the ADC value (blocks take the value from the chart)
- New: block for the measurement of the CPU load
- Improvement: accuracy of the timer
- Improvement: accuracy of the fast counters
- Change: remanence block writes only in the event of a change

V1.0.2.1 (2016-03-11)
- Bugfix: Watchdog (Controllers performed a reboot after one hour, but continue normally now)

V1.0.2.0 (2015-11-19)
- Change: adaption of the hardware with revision B (external reference for voltage measurement)

V1.0.1.0 (2015-10-23)
- New: support of the CAN layer 2 library V2.0 with 29-bit identifier

V1.0.0.1 (2015-09-23)
- 1. Release

STG-680 (ACTIVE – NO DEVELOPMENT)

V1.0.1.2 (2017-10-27)
- New: clock generator 2 (Bugfix for clock generator 1 with slightly changed behavior in macros with the ENABLE block)
- New: Modbus: enhanced setting possibility for parity and number of stop bits (A parity check on the reception does not take place)
- Short flashing of the status LED during power up (on for the duration of initialization)
- Known issue: Timer racing condition - Bug (with 16Bit controller): Clock generator issues no pulse for 66 seconds if the CG block (clock generator) is interrupted exactly while reading the system time stamp by the timer interrupt

V1.0.1.1 (2017-08-09)
- Bugfix: Modbus: multi-slave nets are possible now

V1.0.1.0 (2016-10-19)
- New: reset circuit to clear the program

V1.0.0.1 (2016-08-09)
- Bugfix: converter (float in ...)

V1.0.0.0 (2016-08-03)
- 1. Release

STG-700 (ACTIVE – NO DEVELOPMENT)

V1.0.1.0 (2016-10-19)
- New: reset circuit to clear the program
- Known issue: Timer racing condition - Bug (with 16Bit controller): Clock generator issues no pulse for 66 seconds if the CG block (clock generator) is interrupted exactly while reading the system time stamp by the timer interrupt

V1.0.0.1 (2016-08-09)
- Bugfix: converter (float in ...)

V1.0.0.0 (2016-08-03)
- 1. Release

STG-800/810 (ACTIVE)

V1.01.211215 (V1.1.0.0) (2021-12-15)
- New: Visualization of system voltages that are too low during start-up with the aid of the status LED via the following periodic signal: Rising light for 1 second, then off for 0.5 seconds
- Bugfix: Timer-Init-Bug (time 0.1% too long): System clock has been corrected to 1.000 ms
- Bugfix: High-Resolution-PWM-Bug: The PWM output is now initialized correctly, even if only the special block is used
- Bugfix: CAN-ID 0-Bug: The firmware no longer gets stuck when receiving CAN messages with ID 0 if they are not used by blocks
- Bugfix: Remanence memory write bug: The full remanence and system remanence memory can now be used, even if all signals are changed simultaneously
- Bugfix: Drift in moving average: Possible drift removed, by recalculating the inner sums after each complete run
- Bugfix: System start-up bug (when the minimum voltages are not reached): A correct start after prolonged operation at undervoltage now works
- Improvement: Repeated download of small projects accelerated
- Improvement: Accuracy of the frequency during PWM measurement (Correction by -0.125 ppm)
- Change: Measurement error of the times during PWM measurement symmetrized (from -1 .. 0 µs to -0.5 .. 0.5 µs)

V1.00.180405 (V1.0.1.1) (2018-04-05)
- Bugfix: CAN-status block: output of „Error TX-Message lost“ is possible now in case of an open circuit
- Known issue: CAN-ID 0-Bug: The firmware gets caught in an endless loop when receiving a CAN message with ID 0
- Known issue: High Resolution-PWM-Bug: The PWM output is not working when the special block is used only
- Known issue: Timer-Init-Bug (time 0.1% too long): The 1.000ms internal clock is 1.001ms long (0.1% too long). The task cycle time and all time blocks are affected
- Known issue: Remanence memory write bug: When using the entire remanence memory, the last byte is not written when changes are made, including all bytes that were changed at the same time
- Known issue: System start-up bug (when the minimum voltages are not reached): Control does not reliably start up correctly, even when the supply voltage is OK again

V1.00.180326 (V1.0.1.0) (2018-03-26)
- Bugfix: sporadic reset of the activation removed (triggered by an operation outside the specifications)
- New: usage of the integrated voltage monitoring in order to comply with the specifications (delay during booting or reset when leaving the operation range for a longer period)
- New: system functions for the reading out of a voltage error
- New: system functions for the controlling PWM with a higher resolution and an extended frequency range

V1.00.171127 (V1.0.0.7) (2017-11-27)
- Bugfix: CAN initialization: internal timeout reduced form ~30s to ~20ms
- Bugfix: CAN Tx: timeout, reduced from 10ms per message to a dynamically adopted value (4ms - 0ms)
- Bugfix: CAN Tx queue: fully available now (previously 1 entry was not available)
- Bugfix: status LED now will be deactivated after the download, if it was activated previously
- Bugfix: PWM measurement and encoder function now will be deactivated after the download, if they were activated previously
- Change: status LED flashes at 10Hz during the download
- Change: CAN status block is able to set Bit5 and Bit7 simultaneously -> signaling that the send queue is full (11 messages)
- Change: CAN status block is able to set Bit6 and Bit7 simultaneously -> signaling that at least one message has not been sent (status remains set as long as the sent queue is full)
- Improvement: availability of the controller is significantly improved during high processor load

V1.00.171019 (V1.0.0.6) (2017-10-19)
- New: clock generator 2 (Bugfix for clock generator 1 with slightly changed behavior in macros with the ENABLE block)
- Bugfix: correct CAN status report now even after download
- Restriction with the STG-810: IrDA is not supported

V1.00.170314 (V1.0.0.5) (2017-03-14)
- 1. Release

STG-820 (ACTIVE)

V1.01.211215 (V1.1.0.0) (2021-12-15)
- New: Visualization of system voltages that are too low during start-up with the aid of the status LED via the following periodic signal: Rising light for 1 second, then off for 0.5 seconds
- Bugfix: Timer-Init-Bug (time 0.1% too long): System clock has been corrected to 1.000 ms
- Bugfix: CAN-ID 0-Bug: The firmware no longer gets stuck when receiving CAN messages with ID 0 if they are not used by blocks
- Bugfix: Remanence memory write bug: The full remanence and system remanence memory can now be used, even if all signals are changed simultaneously
- Bugfix: Drift in moving average: Possible drift removed, by recalculating the inner sums after each complete run
- Bugfix: System start-up bug (when the minimum voltages are not reached): A correct start after prolonged operation at undervoltage now works
- Improvement: Repeated download of small projects accelerated
- Improvement: Accuracy of the frequency during PWM measurement (Correction by -0.125 ppm)
- Change: Measurement error of the times during PWM measurement symmetrized (from -1 .. 0 µs to -0.5 .. 0.5 µs)

V1.00.180405 (V1.0.1.1) (2018-04-05)
- Bugfix: CAN-status block: output of „Error TX-Message lost“ is possible now in case of an open circuit
- Known issue: CAN-ID 0 - Bug: The firmware gets caught in an endless loop when receiving a CAN message with ID 0
- Known issue: Timer-Init-Bug (time 0.1% too long): The 1.000ms internal clock is 1.001ms long (0.1% too long). The task cycle time and all time blocks are affected
- Known issue: Remanence memory write bug: When using the entire remanence memory, the last byte is not written when changes are made, including all bytes that were changed at the same time
- Known issue: System start-up bug (when the minimum voltages are not reached): Control does not reliably start up correctly, even when the supply voltage is OK again

V1.00.180326 (V1.0.1.0) (2018-03-26)
- Bugfix: sporadic reset of the activation removed (triggered by an operation outside the specifications)
- New: usage of the integrated voltage monitoring in order to comply with the specifications (delay during booting or reset when leaving the operation range for a longer period)
- New: system functions for the reading out of a voltage error

V1.00.171127 (V1.0.0.1) (2017-11-27)
- Bugfix: CAN initialization: internal timeout reduced form ~30s to ~20ms
- Bugfix: CAN Tx: timeout, reduced from 10ms per message to a dynamically adopted value (4ms - 0ms)
- Bugfix: CAN Tx queue: fully available now (previously 1 entry was not available)
- Bugfix: status LED now will be deactivated after the download, if it was activated previously
- Bugfix: PWM measurement and encoder function now will be deactivated after the download, if they were activated previously
- Change: status LED flashes at 10Hz during the download
- Change: CAN status block is able to set Bit5 and Bit7 simultaneously -> signaling that the send queue is full (11 messages)
- Change: CAN status block is able to set Bit6 and Bit7 simultaneously -> signaling that at least one message has not been sent (status remains set as long as the sent queue is full)
- Improvement: availability of the controller is significantly improved during high processor load

V1.00.171019 (V1.0.0.0) (2017-10-19)
- 1. Release
- New: clock generator 2 (Bugfix for clock generator 1 with slightly changed behavior in macros with the ENABLE block)
- Limitation: IrDA is not supported

STG-850 (ACTIVE)

V1.01.211215 (V1.1.0.0) (2021-12-15)
- New: Visualization of system voltages that are too low during start-up with the aid of the status LED via the following periodic signal: Rising light for 1 second, then off for 0.5 seconds
- Bugfix: Timer-Init-Bug (time 0.1% too long): System clock has been corrected to 1.000 ms
- Bugfix: High-Resolution-PWM-Bug: The PWM output is now initialized correctly, even if only the special block is used
- Bugfix: CAN-ID 0-Bug: The firmware no longer gets stuck when receiving CAN messages with ID 0 if they are not used by blocks
- Bugfix: Remanence memory write bug: The full remanence and system remanence memory can now be used, even if all signals are changed simultaneously
- Bugfix: Drift in moving average: Possible drift removed, by recalculating the inner sums after each complete run
- Bugfix: System start-up bug (when the minimum voltages are not reached): A correct start after prolonged operation at undervoltage now works
- Improvement: Repeated download of small projects accelerated
- Improvement: Accuracy of the frequency during PWM measurement (Correction by -0.125 ppm)
- Change: Measurement error of the times during PWM measurement symmetrized (from -1 .. 0 µs to -0.5 .. 0.5 µs)

V1.00.180405 (V1.0.1.1) (2018-04-05)
- Bugfix: CAN-status block: output of „Error TX-Message lost“ is possible now in case of an open circuit
- Known issue: CAN-ID 0 - Bug: The firmware gets caught in an endless loop when receiving a CAN message with ID 0
- Known issue: High Resolution-PWM-Bug: The PWM output is not working when the special block is used only
- Known issue: Timer-Init-Bug (time 0.1% too long): The 1.000ms internal clock is 1.001ms long (0.1% too long). The task cycle time and all time blocks are affected
- Known issue: Remanence memory write bug: When using the entire remanence memory, the last byte is not written when changes are made, including all bytes that were changed at the same time
- Known issue: System start-up bug (when the minimum voltages are not reached): Control does not reliably start up correctly, even when the supply voltage is OK again

V1.00.180326 (V1.0.1.0) (2018-03-26)
- Bugfix: sporadic reset of the activation removed (triggered by an operation outside the specifications)
- New: usage of the integrated voltage monitoring in order to comply with the specifications (delay during booting or reset when leaving the operation range for a longer period)
- New: system functions for the reading out of a voltage error
- New: system functions for the controlling of the PWM with a higher resolution and an extended frequency range

V1.00.171127 (V1.0.0.2) (2017-11-27)
- Bugfix: CAN initialization: internal timeout reduced form ~30s to ~20ms
- Bugfix: CAN Tx: timeout, reduced from 10ms per message to a dynamically adopted value (4ms - 0ms)
- Bugfix: CAN Tx queue: fully available now (previously 1 entry was not available)
- Bugfix: status LED now will be deactivated after the download, if it was activated previously
- Bugfix: PWM measurement and encoder function now will be deactivated after the download, if they were activated previously
- Change: status LED flashes at 10Hz during the download
- Change: CAN status block is able to set Bit5 and Bit7 simultaneously -> signaling that the send queue is full (11 messages)
- Change: CAN status block is able to set Bit6 and Bit7 simultaneously -> signaling that at least one message has not been sent (status remains set as long as the sent queue is full)
- Improvement: availability of the controller is significantly improved during high processor load

V1.00.171019 (V1.0.0.1) (2017-10-19)
- 1. Release
- New: clock generator 2 (Bugfix for clock generator 1 with slightly changed behavior in macros with the ENABLE block)
- Limitation: IrDA is not supported

STG-860 / WCU860S (OBSOLETE)

V1.01.211215 (V1.1.0.0) (2021-12-15)

- New: Visualization of system voltages that are too low during start-up with the aid of the status LED via the following periodic signal: Rising light for 1 second, then off for 0.5 seconds
- Bugfix: Timer-Init-Bug (time 0.1% too long): System clock has been corrected to 1.000 ms
- Bugfix: High-Resolution-PWM-Bug: The PWM output is now initialized correctly, even if only the special block is used
- Bugfix: CAN-ID 0-Bug: The firmware no longer gets stuck when receiving CAN messages with ID 0 if they are not used by blocks
- Bugfix: Remanence memory write bug: The full remanence and system remanence memory can now be used, even if all signals are changed simultaneously
- Bugfix: Drift in moving average: Possible drift removed, by recalculating the inner sums after each complete run
- Bugfix: System start-up bug (when the minimum voltages are not reached): A correct start after prolonged operation at undervoltage now works
- Improvement: Repeated download of small projects accelerated
- Improvement: Accuracy of the frequency during PWM measurement (Correction by -0.125 ppm)
- Change: Measurement error of the times during PWM measurement symmetrized (from -1 .. 0 µs to -0.5 .. 0.5 µs)

V1.00.180405 (V1.0.1.1) (2018-04-05)

- Bugfix: CAN-status block: output of „Error TX-Message lost“ is possible now in case of an open circuit
- Known issue: CAN-ID 0 - Bug: The firmware gets caught in an endless loop when receiving a CAN message with ID 0
- Known issue: High Resolution-PWM-Bug: The PWM output is not working when the special block is used only
- Known issue: Timer-Init-Bug (time 0.1% too long): The 1.000ms internal clock is 1.001ms long (0.1% too long). The task cycle time and all time blocks are affected
- Known issue: Remanence memory write bug: When using the entire remanence memory, the last byte is not written when changes are made, including all bytes that were changed at the same time
- Known issue: System start-up bug (when the minimum voltages are not reached): Control does not reliably start up correctly, even when the supply voltage is OK again

V1.00.180326 (V1.0.0.0) (2018-03-26)

- 1. Release (is based on the STG-850 and contains all features from 2018-03-26)

TROUBLESHOOTING

1 System start-up Bug (when the minimum voltages are not reached):
- Description: The valid voltage range is monitored and the system start is prevented as long as the voltage is not OK. After 5 seconds, the watchdog triggers a reset and the controller remains in test mode. If the voltage is correct afterwards, the controller goes into stop mode and the application does not start
- Workaround: Perform full power cycle if the application does not start and the supply voltage level is OK
- Controller affected: STG-8XX

2 Remanence memory write bug:
- Description: When using the entire remanence memory, the last byte is not written when changes are made, including all bytes that were changed at the same time
- Workaround: Maximum use of 127 instead of 128 bytes from normal remanence memory and only 63 instead of 64 bytes from system remanence memory
- Controller affected: STG-8XX

3 CAN-ID 0 - Bug:
- Description: Firmware gets stuck in an infinite loop when receiving a CAN message with ID 0
- Workaround 1: Use an even number of CAN receive blocks (regardless of whether 11 or 29 Bit)
- Workaround 2: Use a CAN-Rx block (11 Bit) with ID 0 or 0x000
- Controller affected: STG-8XX

4 High Resolution-PWM-Bug:
- Description: The PWM output does not work if only the special block is used
- Workaround: The PWM output can be initialized by the correct single usage of the normal PWM block. Then, the usage of the high resolution PWM is possible
- Controller affected: STG-8XX

5 Timer racing condition Bug (with 16bit Controller):
- Description: Clock generator does not output a pulse for 66 seconds if the CG block (clock generator) is interrupted by the timer interrupt exactly when reading the system timestamp
- Recommendation: no usage of the time blocks in critical application (Problem occurs only very rarely, but is not excluded)
- Workaround: replacement of the time function by replication with blocks over counting of application cycles
- Controller affected: STG-32/115/5XX/6XX/700

6 Timer-Init-Bug (time 0.1% too long):
- Description: The 1.000 ms system clock is 1.001 ms long (0.1% too long). The task cycle time and all time blocks are affected
- Workaround: Adjustment of time values to 99.9 percent of the actual value
- Note: Task cycle time only conditionally correctable
- Assessment: effect notable only during long-term measurements
- Controller affected: STG-8XX